

## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.

9797-050-999

APPLICATION NO.

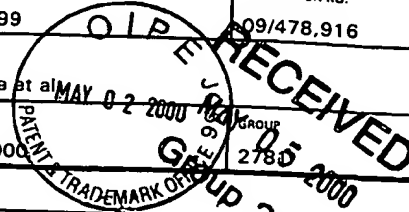
09/478,916

APPLICANT

Jared L. Zerbe et al.

FILING DATE

January 6, 2000



## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
W	AA	5,194,765	Mar. 16, 1993	Dunlop et al.	307	443	Jun 28, 1991
	AB	5,254,883	Oct. 19, 1993	Horowitz et al.	307	443	Apr 22, 1992
	AC	5,513,327	Apr. 30, 1996	Farmwald et al.	395	309	Mar 31, 1994
	AD	5,023,488	Jun. 11, 1991	Gunning	307	475	Mar 30, 1990
	AE	5,483,110	Jan. 9, 1996	Koide et al.	307	147	Feb 28, 1994
	AF	5,287,108	Feb. 15, 1994	Mayes et al.	341	156	Jul 2, 1992
W	AG	5,977,798	Nov. 2, 1999	Zerbe	326	98	Jul 18, 1997

## FOREIGN PATENT DOCUMENTS

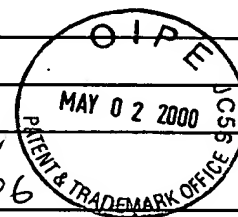
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO
W	AH	EP 0 463 316 A1	02 Jan 92	DE FR GB	H04L	12/40	X
W	AI	EP 0 482 392 A2	29 Apr 92	AT BE CH DE DK ES FR GB IT LI NL SE	H04L	25/08	X
W	AJ	58-54412 (A)	31 Mar 83	JP	G05F1	56	

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

W	AK	Sidiropoulos, Stefanos et al.; "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers"; IEEE Journal of Solid-State Circuits; Vol. 32, No. 5, May 1997; pp. 681-690.
	AL	Donnelly, Kevin S et al.; "A 660 MB/s Interface Megacell Portable Circuit in 0.3 $\mu$ m-0.7 $\mu$ m CMOS ASIC"; IEEE Journal of Solid State Circuits; Vol. 31, No. 12; December 1996, pp. 1995-2003.
	AM	Allen, Arnold O.; "Probability, Statistics, and Queueing Theory with Computer Science Applications"; 2 <sup>nd</sup> Edition, CH 7; pp. 450, 458-459.
	AN	Chappell, Terry I. et al.; "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM"; IEEE International Solid State Circuits Conference 1991; pp. 50-51.
	AO	Pilo, Harold et al.; "A 300 MHz 3.3V 1 Mb SRAM Fabricated in a 0.5 $\mu$ m CMOS Process"; IEEE International Solid State Circuits Conference 1996; pp. 148-149.
	AP	Schumacher, Hans-Jürgen et al.; "CMOS Subnanosecond True-ECL Output Buffer"; IEEE Journal of Solid-State Circuits; Vol. 25, No. 1; February 1990 pp. 150-154.
	AQ	Yang, Tsen-Shau et al.; "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM"; IEEE Journal of D-State Circuits; Vol. 23, No. 5; October 1988; pp. 1030-1040.
W	AR	S. Sidiropoulos et al., "A 700 Mb/s/pin CMOS Signalling Interface Using Current Integrating Receivers", IEEE VLSI Circuits Symposium, 1996; pp. 142-143.

we	AS	M. Bazes, " <u>Two Novel Fully complementary Self-Biased CMOS Differential Amplifiers</u> ", IEEE Journal of Solid State Circuits, Vol. 26 No. 2, February 1991.
	AT	M. Ishibe et al., " <u>High-Speed CMOS I/O Buffer Circuits</u> ", IEEE Journal of Solid State Circuits, Vol. 27, No. 4, April 1992.
	AU	J. Lee et al., " <u>A 80ns 5v-Only Dynamic RAM</u> ", ISSCC proceedings, Paper 12.3, ISSCC 1979.
	AV	T. Seki et al., " <u>A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier</u> ", IEEE Journal of Solid State Circuits, Vol. 28, No. 4., April 1993.
	AW	T. Kobayashi et al., " <u>A current-controlled latch sense amplifier and a static power-saving input buffer for low-pressure architecture</u> ", IEEE Journal of Solid State Circuits Vol. 28 No. 4., April 1993.
	AX	L. Tomasini et. al., " <u>A fully differential CMOS line driver for ISDN</u> ", IEEE Journal of Solid State Circuits, Vol. 25, No. 2., April 1990.
	AY	R. Farjad-Rad et al., " <u>A 0.4-um CMOS 10-Gb/s 4-PAM pre-emphasis serial link transmitter</u> ", IEEE J. Solid-State Circuits, Vol. No. 34, pp. 580-585, May 1999.
	AZ	E. Yeung et al., " <u>A 2.4Gbps per pin simultaneous bidirectional parallel link with per pin skew calibration</u> ", ISSCC 2000, in press as of 1-9-2000.
	BA	C. Portmann et al., " <u>A multiple vendor 2.5-V DLL for 1.6-GB/s RDRAMs</u> ", IEEE VLSI Circuits Symposium, June 1999.
	BB	A. Moncayo et al., " <u>Bus design and analysis at 500MHz and beyond</u> ", Presented at the Design SuperCon, 1995.
we	BC	B. Lau et al., " <u>A 2.6-Gbyte/s multipurpose chip-to-chip interface</u> ", IEEE J. Solid-State Circuits, Vol. 33, pp. 1617-1626, November 1998.
EXAMINER	DATE CONSIDERED	
	1/5/06	

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.





## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.

009797-0050-999

APPLICATION NO.

09/478,916

APPLICANT

Zerbe et al.

FILING DATE

January 6, 2000

GROUP

2781

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
we	AA	4,280,221	Jul. 21, 1981	Chun et al.			
	AB	4,620,188	Oct. 28, 1986	Sengchanh			
	AC	4,825,450	Apr. 25, 1989	Herzog			
	AD	5,259,002	Nov. 2, 1993	Carlstedt			
	AE	5,412,689	May 2, 1995	Chan et al.			
	AF	5,553,097	Sep. 3, 1996	Dagher			
	AG	5,644,253	Jul. 1, 1997	Takatsu			
	AH	5,761,246	Jun. 2, 1998	Cao et al.			
	AI	5,864,584	Jan. 26, 1999	Cao et al.			
we	AJ	6,005,895	Dec. 21, 1999	Perino et al.			

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
we	AK	EP 0 352 869 A2	Jul. 27, 1989	EPO (Shell Internationale Research Maatschappij B.V.)				
we	AL	WO 95/31867	Nov. 23, 1995	PCT (Bell Communications Research, Inc.)				
	AM							
	AN							
	AO							

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

we	AP	Scott; "Propagation Over Multiple Parallel Transmission Lines Via Modes"; IBM Technical Disclosure Bulletin, U.S.; Vol. 32, NR. 11, April 1990.
we	AQ	Taborek; "Multi-Level Analog Signaling Techniques for 10 Gigabit Ethernet"; IEEE 802.3 Tutorial.
	AR	

EXAMINER

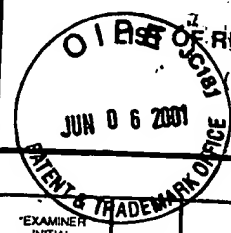
Luis J. S.

DATE CONSIDERED

1/5/06

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

06-08-01 #6/Prior Art  
 Sheet 1 of 5  
 T. McBeath-Brown



REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO. 9797-0050-999		APPLICATION NO. 09/478,916
APPLICANT Zerbe et al.		
FILING DATE January 6, 2000		GROUP 2781

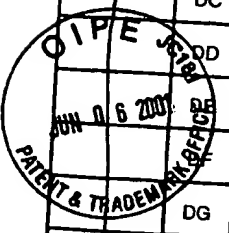
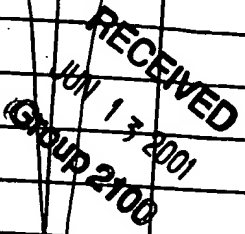
U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
W	AR Re 30,182	12/25/79	Howson			
	AS 2,912,684	11/10/59	Steele			
	AT 3,051,901	08/28/62	Yaeger			
	AU 3,078,378	02/19/63	Burley et al.			
	AV 3,267,459	08/16/66	Chomicki et al.			
	AW 3,484,559	12/16/69	Rigby			
	AX 3,508,076	04/21/70	Winder			
	AY 3,510,585	05/05/70	Stone			
	AZ 3,560,856	02/02/71	Kaneko			
	BA 3,569,955	03/09/71	Maniere			
	BB 3,571,725	03/23/71	Kaneko et al.			
	BC 3,587,088	06/22/71	Franaszek			
	BD 3,648,064	03/07/72	Mukai et al.			
	BE 3,697,874	10/10/72	Kaneko			
	BF 3,731,199	05/01/73	Tazaki et al.			
	BG 3,733,550	05/15/73	Tazaki et al.			
	BH 3,753,113	08/14/73	Maruta et al.			
	BI 3,754,237	08/21/73	de Laage de Meux			
	BJ 3,761,818	09/25/73	Tazaki et al.			
	BK 3,772,680	11/13/73	Kawai et al.			
	BL 3,798,544	03/19/74	Norman			
	BM 3,832,490	08/27/74	Leonard			
	BN 3,860,871	01/14/75	Hinoshita et al.			
	BO 3,876,944	04/08/75	Mack et al.			
	BP 3,927,401	12/16/75	McIntosh			
	BQ 3,978,284	08/31/76	Yoshino et al.			
	BR 3,988,676	10/26/76	Whang			
	BS 4,038,564	07/26/77	Hakata			
W	BT 4,070,650	01/24/78	Ohashi et al.			

RECEIVED  
 JUN 13 2001  
 Group 2100

BU	4,086,587	04/25/78	Lender
BV	4,097,859	06/27/78	Looschen
BW	4,131,761	12/26/78	Giusto
BX	4,181,865	01/01/80	Kohyama
BY	4,373,152	02/08/83	Jacobsthal
BZ	4,382,249	05/03/83	Jacobsthal
CA	4,403,330	09/06/83	Meyer
CB	4,408,135	10/04/83	Yuyama et al.
CC	4,408,189	10/04/83	Betts et al.
CD-1	4,528,550	07/09/85	Graves et al.
CD-2	4,438,491	03/20/84	Constant
CE	4,571,735	02/18/96	Furse
CF	4,602,374	07/22/86	Nakamura et al.
CG	4,628,297	12/09/86	Mita et al.
CH	4,779,073	10/18/88	Iketani
CI	4,805,190	02/14/89	Jaffre et al.
CJ	4,821,286	04/11/89	Graczyk et al.
CK	4,823,028	04/18/89	Lloyd
CL	4,841,301	06/20/89	Ichihara
CM	4,860,309	08/22/89	Costello
CN	4,875,049	10/17/89	Yoshida
CO	4,888,764	12/19/89	Haug
CP	5,003,555	03/26/91	Bergmans
CQ	5,045,728	09/03/91	Crafts
CR	5,115,450	05/19/92	Arcuri
CS	5,121,411	06/09/92	Fluharty
CT	5,172,338	12/15/92	Mehrotra et al.
CU	5,191,330	03/02/93	Fisher et al.
CV	5,230,008	07/20/93	Duch et al.
CW	5,243,625	09/07/93	Verbakel et al.
CX	5,280,500	01/18/94	Mazzola et al.
CY	5,295,155	03/15/94	Gersbach et al.
CZ	5,315,175	05/24/94	Langner
DA	5,331,320	07/19/94	Cideciyan et al.

*W*

DB	5,408,498	04/18/95	Yoshida
DC	5,425,056	06/13/95	Maroun et al.
DD	5,426,739	06/20/95	Lin et al.
DE	5,438,593	08/01/95	Karam et al.
DF	5,459,749	10/17/95	Park
DG	5,471,156	11/28/95	Kim et al.
DH	5,473,635	12/05/95	Chevroulet
DI	5,525,983	06/11/96	Patel et al.
DJ	5,633,631	05/27/97	Techman
DK	5,640,605	06/17/97	Johnson et al.
DL	5,684,833	11/04/97	Watanabe
DM	5,740,201	04/14/98	Hui
DN	5,793,815	08/11/98	Goodnow et al.
DO	5,793,816	08/11/98	Hui
DP	5,796,781	08/18/98	DeAndrea et al.
DQ	5,825,825	10/20/98	Altmann et al.
DR	5,872,468	02/16/99	Dyke
DS	5,892,466	04/06/99	Walker
DT	5,898,734	04/27/99	Nakamura et al.
DU	5,917,340	06/29/99	Manohar et al.
DV	5,933,458	08/03/99	Leurent et al.
DW	5,942,994	08/24/99	Lewiner et al.
DX	5,946,355	08/31/99	Baker
DY	5,949,280	09/07/99	Sasaki
DZ	5,969,579	10/19/99	Hartke et al.
EA	5,969,648	10/19/99	Garnett
EB	6,018,550	01/25/00	Emma et al.
EC	6,038,260	03/14/00	Emma et al.
ED	6,049,229	04/11/00	Manohar et al.
EE	6,052,390	04/18/00	Deliot et al.
EF	6,067,326	05/23/00	Johsson et al.
EG	6,078,627	06/20/00	Crayford
EH	6,084,931	07/04/00	Powell, II et al.
<i>W</i> EI	6,094,461	07/25/00	Heron

W	EJ	6,101,561	08/08/00	Beers et al.				
	EK	6,114,979	09/05/00	Kim				
		6,122,010	09/19/00	Emelko				
		6,140,841	10/31/00	Suh				
	EN	6,195,397 B1	02/27/01	Kwon				

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
W	EO	DE 43 20 930	01/05/95	Germany (Kommunikations Elektronik)				
	EP	EP 0 094 624	11/23/83	EPO (Siemens AG)				
	EQ	EP 0 490 504 A2	06/07/92	EPO (Northern Telecom Limited)				
	ER	JP 54051343	04/23/79	Japan (Hitachi Ltd)				
	ES	JP 56164650	12/17/81	Japan (Toshiba Corp)				
	ET	JP 59036465	02/28/84	Japan (Sony Corp)				
	EU	JP 60087551	05/17/85	Japan (Fujitsu Ltd.)				
	EV	JP 60194647	10/03/85	Japan (Hitachi Ltd)				
	EW	JP 02128201	05/16/90	Japan (Fuji Electric Co Ltd)				
	EX	JP 02140676	05/30/90	Japan (Advantest Corp)				
	EY	JP 04044691	02/14/92	Japan (Seiko Instr Inc)				
	EZ	JP 05143211	06/11/93	Japan (Omron Corp)				
	FA	JP 08202677	08/09/96	Japan (Mitsubishi Electric Corp)				
	FB	JP 08286943	11/01/96	Japan (Takaoka Electric Mfg Co Ltd)				
	FC	JP 09181778	07/11/97	Japan (Aiphone Co Ltd)				
	FD	WO 96/31038	10/03/96	PCT (Hitachi Ltd)				
W	FE	WO 98/33306	07/30/98	PCT (Fukuda)				

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

W	FF	Current, 1994, "Current-mode CMOS multiple-valued logic circuits," <u>IEEE Journal of Solid-State Circuits</u> 29(2):95-107
	FG	Dally and Poulton, <u>Digital Systems Engineering</u> , Cambridge University Press, New York, NY, 1998, pp. 344-347 and 352.
	FH	Farjad-Rad <i>et al.</i> , "An equalization scheme for 10Gb/s 4-PAM signaling over long cables," Presentation. Center for Integrated Systems, Department of Electrical Engineering, Stanford University, July 28, 1997.
	FI	Farjad-Rad <i>et al.</i> , 1999, "A 0.4- $\mu$ m CMOS 10-GB/s 4-PAM pre-emphasis serial link transmitter," <u>IEEE Journal of Solid-State Circuits</u> 34(5):580-585
	FJ	IBM Technical Disclosure Bulletin, June 1967, "Use of multibit encoding to increase linear recording densities in serially recorded records," pp. 14-15
	FK	IBM Technical Disclosure Bulletin, Jan. 1968, "Coding data transmission," pp. 1295-1296
W	FL	IBM Technical Disclosure Bulletin, July 1969, "Clock recovery circuit," pp. 219-220

W	FM	IBM Technical Disclosure Bulletin, Nov. 1970, "Transmission by data encoding," pp. 1519-1520
	FN	IBM Technical Disclosure Bulletin, Feb. 1976, "Bidirectional communications within a binary switching system," pp. 2865-2866
	FO	IBM Technical Disclosure Bulletin, Feb. 1976, "Multilevel bidirectional signal transmission," pp. 2867-2868
	FP	IBM Technical Disclosure Bulletin, Oct. 1978, "Multilevel signal transfers," pp. 1798-1800
		IBM Technical Disclosure Bulletin, Feb. 1981, "Circuit for multilevel logic implementation," pp. 4206-4209
	FR	IBM Technical Disclosure Bulletin, April 1983, "Multi level logic testing," pp. 5903-5904
	FS	IBM Technical Disclosure Bulletin, Sept. 1985, "Push-pull multi-level driver circuit for input-output bus," pp. 1649-1651
	FT	IBM Technical Disclosure Bulletin, Aug. 1986, "Multilevel CMOS sense amplifier," pp. 1280-1281
	FU	IBM Technical Disclosure Bulletin, Nov. 1992, "Multi-level encoded high bandwidth bus," pp. 444-447
	FV	IBM Technical Disclosure Bulletin, Feb 1995, "High speed complimentary metal oxide semiconductor input/output circuits," pp. 111-114
	FW	IBM Technical Disclosure Bulletin, April 1995, "Common front end bus for high-performance chip-to-chip communication," pp. 443-444
	FX	IBM Technical Disclosure Bulletin, April 1995, "High performance impedance controlled CMOS Drive," pp. 445-448
	FY	IBM Technical Disclosure Bulletin, April 1995, "3-state decoder for external 3-state buffer," pp. 477-478
	FZ	Matick, <u>Transmission Lines for Digital and Communication Networks: An Introduction to Transmission Lines, High-frequency and High-speed Pulse Characteristics and Applications</u> , IEEE Press, New York, NY, 1995, pp. 268-269.
	GA	Singh, 1987, "Four valued buses for clocked CMOS VLSI systems," <u>Proceedings of the Seventeenth International Symposium on Multiple-Valued Logic</u> , The Computer Society of the IEEE. Boston, Massachusetts, May 26-28, 1987, pp. 128-133
	GB	Smith, 1981, "The prospects for multivalued logic: A technology and applications view," <u>IEEE Transactions on Computers</u> C-30(9):619-634
	GC	Thirion, "10 Gig PMD Technologies," <u>IEEE Plenary</u> , Kauai, Hawaii, November 1999.
W	GD	Vranesic, 1979, "Multivalued signaling in daisy chain bus control," <u>Proceedings of the Ninth International Symposium on Multiple-Valued Logic</u> , Bath, England, pp. 14-18.

EXAMINER

DATE CONSIDERED

1/5/06

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

RECEIVED  
JUN 13 2001  
Group 2100



#7



## LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.

9797-0050-999

APPLICATION NO.

09/478,916

APPLICANT

Zerbe et al.

FILING DATE

January 6, 2000

GROUP

2781

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

RECEIVED  
JUL 30 2001  
Technology Center 2100

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
we	JP60191231	8/30/85	Japan			X	
we	JP56168711	10/23/81	Japan			X	
we	JP52127887	10/24/77	Japan			X	

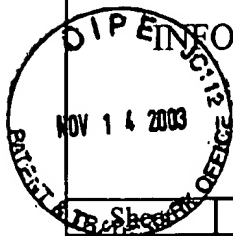
## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)


EXAMINER

DATE CONSIDERED

1/5/06

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



INFORMATION DISCLOSURE CITATION				Complete If Known	
PTO-1449				Application Number	09/478,916
				Filing Date	January 6, 2000
				First Named Inventor	Jared L. Zerbe et al.
				Art Unit	2189
				Examiner Name	Tim T. Vo
				Attorney Docket Number	9797-0050-999

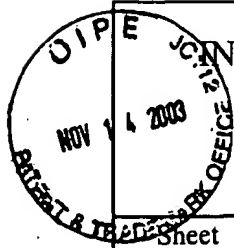
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
me	US 2001/0010712 A1	8/2/01	Hedberg			
	US 2001/0016929 A1	8/23/01	Bonneau et al.			
	US 2001/0019584 A1	9/6/01	Azazzi et al.			
	US 2001/0021987 A1	9/13/01	Govindarajan et al			
	4,481,625	11/6/84	Roberts et al.			
	4,748,637	5/31/88	Bishop et al.			
	5,023,841	6/11/91	Akrout et al.			
	5,046,050	9/3/91	Kertis			
	5,126,974	6/30/92	Sasaki et al.			
	5,153,459	10/6/92	Park et al.			
	5,295,157	3/15/94	Suzuki et al.			
	5,373,473	12/13/94	Okumura			
	5,508,570	4/16/96	Laber et al.			
	5,534,795	7/9/96	Wert et al.			
	5,534,798	7/9/96	Phillips et al.			
	5,539,774	7/23/96	Nobakht et al.			
	5,546,042	8/13/96	Tedrow et al.			
	5,596,439	1/21/97	Dankberg et al.			
	5,604,468	2/18/97	Gillig			
	5,604,605	2/18/97	Moolenaar			
	5,608,755	3/4/97	Rakib			
	5,663,663	9/2/97	Cao et al.			
	5,694,424	12/2/97	Ariyavisitakul			
	5,734,294	3/31/98	Bezzam et al.			
	5,742,591	4/21/98	Himayat et al.			
me	5,751,168	5/12/98	Speed, III et al.			

Examiner Signature	<i>Tim T. Vo</i>	Date Considered	11/5/06
--------------------	------------------	-----------------	---------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>2</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>3</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>4</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>5</sup> Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



# INFORMATION DISCLOSURE CITATION

PTO-1449

## Complete If Known

Application Number	09/478,916
Filing Date	January 6, 2000
First Named Inventor	Jared L. Zerbe et al.
Art Unit	2189
Examiner Name	Tim T. Vo
Attorney Docket Number	9797-0050-999

Sheet 2 of 4

<i>we</i>	5,757,712	5/26/98	Nagel et al.			
	5,798,918	8/25/98	Georgiou et al.			
	5,809,033	9/15/98	Turner et al.			
	5,852,637	12/22/98	Brown et al.			
	5,887,032	3/23/99	Cioffi			
	5,917,856	6/29/99	Torsti			
	5,970,088	10/19/99	Chen			
	5,973,508	10/26/99	Nowak et al.			
	5,982,741	11/9/99	Ethier			
	5,986,472	11/16/99	Hinedi et al.			
	6,006,169	12/21/99	Sandhu et al.			
	6,009,120	12/28/99	Nobakht			
	6,034,993	3/7/00	Norrell et al.			
	6,037,824	3/14/00	Takahashi			
	6,038,264	3/14/00	Useugi			
	6,048,931	4/11/00	Fujita et al.			
	6,061,395	5/9/00	Tonami			
	6,088,400	7/11/00	Abe			
	6,094,075	7/25/00	Garrett, Jr., et al.			
	6,097,215	8/1/00	Bialas, Jr., et al.			
	6,101,561	8/8/00	Beers et al.			
	6,160,421	12/12/00	Barna			
	6,181,740	1/30/01	Yasuda			
	6,204,785	3/20/01	Fattaruso et al.			
	6,215,635	4/10/01	Nguyen			
	6,222,380	4/24/01	Gerowitz et al.			
<i>we</i>	6,262,611	7/17/01	Takeuchi			

RECEIVED

NOV 20 2003

Technology Center 2100

Examiner  
Signature

*Tim T. Vo*

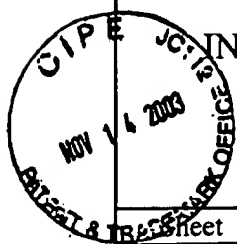
Date  
Considered

1/5/06

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>2</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>3</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>4</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>5</sup> Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



INFORMATION DISCLOSURE  
CITATION

PTO-1449

Complete If Known

Application Number	09/478,916
Filing Date	January 6, 2000
First Named Inventor	Jared L. Zerbe et al.
Art Unit	2189
Examiner Name	Tim T. Vo
Attorney Docket Number	9797-0050-999

Sheet	3	of	4
-------	---	----	---

<i>we</i>	6,275,540	8/14/01	Barrett, Jr., et al.	<b>RECEIVED</b> NOV 20 2003 Technology Center 2100
	6,282,184	8/28/01	Lehman et al.	
	6,289,045 B1	9/11/01	Hasegawa et al.	
	6,307,824	10/23/01	Kuroda et al.	
	6,307,906	10/23/01	Tanji et al.	
	6,373,911	4/16/02	Tajima et al.	
	6,396,329	5/28/02	Zerbe	
<i>we</i>	6,397,408	6/4/02	Veloskey et al.	

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
YES	NO						
<i>we</i>		JP10200345	7/31/98	Japan			X
<i>we</i>		WO 98/33306	7/30/98	WIPO			X
<i>we</i>		WO 99/10982	3/4/99	WIPO			

<i>we</i>	Ariyavisitakul, S., "Reduced-Complexity Equalization Techniques for broadband wireless Channels," (1997), <i>IEEE Journal on Selected Areas in Communications</i> , 15(1), pp. 5-15.
	Ariyavisitakul, S., et al., "Tap-Selectable Decision-Feedback Equalization," (1997), <i>IEEE Transactions on Communications</i> , Vol. 45(12), pp. 1497-1500.
	Azdet, K., et al., "A Gigabit Transceiver Chip Set for UTP CAT-6 Cables in Digital CMOS Technology," (2000), <i>IEEE International Solid State Circuits Conference</i> , pp. 306-307.
	Cova, S.D., et al., "Characterization of Individual Weights in Transversal Filters and Application to CCD's," (1982), <i>IEEE Journal of Solid State Circuits</i> , SC17(6), pp. 1054-1061.
	Dally, W.J., et al., "Multi-gigabit Signaling with CMOS," (5/12/97), <i>DARPA funded presentation</i> , (22 pages).
<i>we</i>	Fiedler, A., et al., "A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis," (2/1997), <i>IEEE/ISSCC</i> .

Examiner Signature	<i>Lin Sh</i>	Date Considered	1/5/06
--------------------	---------------	-----------------	--------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>2</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>3</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>4</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>5</sup> Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



INFORMATION DISCLOSURE  
CITATION

PTO-1449

Complete If Known

Application Number	09/478,916
Filing Date	January 6, 2000
First Named Inventor	Jared L. Zerbe et al.
Art Unit	2189
Examiner Name	Tim T. Vo
Attorney Docket Number	9797-0050-999

Sheet	4	of	4
-------	---	----	---

<i>we</i>	Kuczynski, M.A., et al., "A 1Mb/s Digital Subscriber Line Transceiver Signal Processor," (1999), <i>IEEE Digital and Video Signal Processing/ISSCC</i> , pp. 26-32,
	Perez-Alvarez, I.A., et al., "A Differential Error Reference Adaptive Echo Canceller for Multilevel PAM Line Codes," (1996), <i>IEEE</i> , pp. 1707-1710.
	Raghavan, S.A., et al., "Nonuniformly Spaced Tapped-Delay-Line Equalizers," (1993), <i>IEEE Transactions on Communications</i> , 41(9), pp. 1290-1295.
	Thompson, G., "How 1000BASE-T Works," (1997), <i>Presentation at IEEE 802.3 Plenary Session</i> , (7 pages).
	Yang, K., et al., "A Scalable 32Gb/s Parallel Data Transceiver with On-Chip Timing Calibration Circuits," (2000), <i>IEEE International Solid State Circuits Conference</i> , pp. 258-259.
	"4 Modulation Schemes for High Bit Rate Data Transmission in the Loop Plant," (4/19/01), <a href="http://www.bib.frilippe.de/voltext/dipl/schlegd/chapter4.htm">www.bib.frilippe.de/voltext/dipl/schlegd/chapter4.htm</a> .
	"Propagation Over Multiple Parallel Transmission Lines Via Modes," IBM Technical Disclosure Bulletin, (April 1990). pp. 1-6.
	"Servo Control of Analog Power Supplies Purpose Interface Card," IBM Technical Disclosure Bulletin (April 1993), pp. 1-5 (Vol. 36, Issue 4, pages 283-286).
	IEEE - 802.3ab - A Tutorial Presentation, March 1998.
<i>we</i>	IEEE - P802.3ad-Draft Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method & Physical Layer Specifications: Link Aggregation," (1999).

Examiner Signature	<i>Tim Vo</i>	Date Considered	<i>1/5/06</i>
--------------------	---------------	-----------------	---------------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>2</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>3</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>4</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>5</sup> Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

CA1: 355925.1

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☒ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**